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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re U.S. Patent Application

Applicants: Kurosawa et al.

Serial No. 10/612,414

Filed: July 2, 2003

For: THIN FILM TRANSISTOR DEVICE AND)
 METHOD OF MANUFACTURING THE SAME,)
 THIN FILM TRANSISTOR SUBSTRATE AND)
 DISPLAY HAVING THE SAME)

Art Unit: 2826

Examiner: Erdem, Fazli

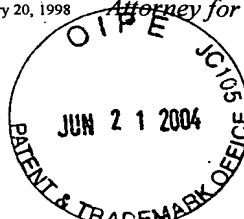
I hereby certify that this paper is being deposited with the United States Postal Service as FIRST-CLASS mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this date.

17 June 04
 Date
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Registration No. 29,367

Appr. February 20, 1998

Attorney for Applicant

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

Dear Sir:

This IDS is submitted under 37 C.F.R. §1.97(c), after the C.F.R. §1.97(b) time period, but before the mail date of a Final Office Action or a Notice of Allowance (whichever occurs first), with either:

- (a) a statement under 37 C.F.R. §1.97(e); or
- (b) the \$180.00 fee under 37 C.F.R. §1.17(p).

Applicant(s) submit herewith Form PTO-1449 (Information Disclosure Citation) together with copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 C.F.R. §1.56. Applicant(s) respectfully submit that the citation of any reference on Form PTO-1449 does not constitute an admission that the reference qualifies as prior art.

It is requested that the information disclosed on the enclosed Form PTO-1449 be made of record in this application.

(X) Statement Under 37 C.F.R. §1.97(e):

(X) The enclosed references were cited in a Communication issued by the Taiwan Patent Office (copy enclosed). Applicant(s) hereby certify that each item of information cited on the enclosed Form PTO-1449 was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three (3) months prior to the filing of this Information Disclosure Statement.

The Commissioner is hereby authorized to charge any additional fees which may be required to this application under 37 C.F.R. §§1.16-1.17, or to credit any overpayment, to Deposit Account No. 07-2069. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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By:

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Form PTO-1449 (Rev. 8-88)	U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No.: 1324.68134	Serial No.: 10/612,414
INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)		Applicant: Kurosawa et al.	
		Filing Date: 07/02/2003	Group: 2826

U.S. PATENT DOCUMENTS

Examiner Initial*	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	6,225,150	May 1, 2001	Lee et al.			
	5,055,899	Oct. 8, 1991	Wakai et al.			
	5,166,085	Nov. 24, 1992	Wakai et al.			
	5,877,514	Mar. 2, 1999	Seo			
	5,969,377	Oct. 19, 1999	Seo			
	6,225,644	May 1, 2001	Yamaguchi et al.			

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
	0 361 609	Apr. 4, 1990	Europe			X	
	2-224254	Sep. 6, 1990	Japan			Abs.	
	60-160170	Aug. 21, 1985	Japan			Abs.	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner

Date Considered

*Examiner:

Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

(ENGLISH TRANSLATION)

OFFICIAL LETTER

Ref. No.: Chichuan No.093203463

Date of Receipt: April 22, 2004

From: THE INTELLECTUAL PROPERTY BUREAU

MINISTRY OF ECONOMIC AFFAIRS

To: FUJITSU DISPLAY TECHNOLOGIES CORPORATION

c/o: PATRICK I.C. YUN AND WILLIAM W.L. CHEN, patent attorneys

SUBJECT:

It is found, upon examination of patent application no. 092118321, that clarifications in some aspects (as indicated hereunder) are still necessary. The applicant is invited to submit, in duplicate, supplementary explanation (along with any amendment) and rebuttal evidence within sixty (60) days of the day following the date of receipt of this Official Letter. **This deadline cannot be extended.** Failure to comply with the requirement, or a late reply to this Letter, will result in the rejection of this application.

CONTENTS:

(Translator's note: Translation of this part is omitted, since this part is concerned merely with the formality requirements for any documents to be submitted.)

If the applicant would like to have a personal interview or demonstration with the Examiner, a request therefor should be made in the Response. If deemed necessary, the time and venue for holding the interview will be arranged.

The Examiner is of the opinion that:

1. The invention relates to a TFT device, a method of manufacturing the same, and a display having the same.
2. The method of manufacturing a thin film transistor device of this invention comprises the formation of a metal layer, a gate insulation layer, a semiconductor layer and a substrate in an order from the top to the bottom, wherein the metal thin film is patterned so as to remove the metal thin film on the semiconductor layer in regions to become source and drain regions of a thin film transistor of a first conductivity type; and then the source and drain regions of the thin film transistor of the first conductivity type are formed by implanting an impurity of the first conductivity type in the semiconductor layer using the patterned metal thin film as a mask; and thereafter, the patterned metal thin film is further patterned. This invention involves the implantation of phosphorus into transistors using the patterned metal thin film as a mask, such that the transistors obtained thereby exhibit good characteristics and high reliability.
3. However, the technologies concerning the formation of each of the layers and the implantation in the manufacture of TFT are well known, as evidenced by US 5055899, US 5166085, US 5877514, US 5969377, US 6225150, US6225644, EP 0361609, JP A02224254 and JP A60160170. Therefore, this invention, which merely comprises the utilization of technology and knowledge existing prior to the filing date and is readily achievable by those skilled in the art, does not meet the patentability requirements. In addition, the examples given in the specification are provided with details on manufacturing the TFT without any solid data demonstrating the advantageous characteristics and reliability thereof. Thus, this invention is devoid of inventive step and does not meet the patentability requirements.
4. Attached hereto is copies of the cited references.

Sealed by
The Intellectual Property Bureau
Ministry of Economic Affairs

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正本

經濟部智慧財產局專利申請案核駁理由先行通知書

受文者：富士通顯示技術股份有限公司（代理人：陳振祥先生、陳文即先生）

地址：臺北市松山區南京東路三段二四八號七樓

發文日期：中華民國九十三年四月十九日

發文文號：第（九三）智專二（六）〇二五五號
第〇九三二〇三四六一三〇號

主旨：第〇九二一一八三二一號專利申請案經審查後發現尚有如說明三所述不明確之處，台端（貴公司）若有具體反證資料或說明，請於文到次日起六十日內提出申復說明及有關反證資料一式二份。若屆期未依通知內容辦理者，專利專責機關得依現有資料續行審查，請查照。

說明：

- 一、本案如有修正應依專利法第四十四條、第四十四條之一、第一百零二條之一、專利法施行細則第二十八條及本局九十一年十一月八日智法字第〇九一八六〇〇一一八—〇號公告之規定辦理並繳修正規費新台幣一千元正（如有補充、修正說明書或圖式者，應備具補充、修正申請書一式二份，並檢送補充、修正部份劃線之說明書或圖式修正頁一式二份及補充、修正後無劃線之說明書或圖式皆換頁一式三份；如補充、修正後致原說明書或圖式頁數不連續者，應檢附補充、修正後之全份說明書或圖式一式三份至局）。
- 二、若希望來局當面示範或說明，請於申復說明書內註明「申請面詢」，本局認為有必要時，另安排地點、時間舉辦「面詢」，並繳交規費新台幣二千元正。
- 三、本案經審查認為：
 - （一）本案「薄膜電晶體裝置及其製造方法，薄膜電晶體基材及具有此基材之顯示器」之要點在

第一頁

於提供一種顯示裝置，及其製造方法，與及由此顯示裝置所製造之顯示器。

- （二）本案顯示裝置之製造方法包括由上而下依序為金屬薄膜、閘極絕緣層薄膜、半導體層及基材上，而在金屬薄膜形成圖案，以去除在欲成為第一導電型之顯示裝置之源極與汲極區域之區域內之半導體層上的金屬薄膜，再藉由第一導電型之線質植入使用該圖案化之金屬薄膜作為罩膜的半導體層內而形成該第一導電型之薄膜之顯示裝置之源極及汲極區域，同時，再藉由該已圖案化之金屬薄膜形成圖案等步驟而成，而本案乃利用植入技術，使用該圖案化之金屬薄膜作為罩膜而將矽離子植入，據謂可獲得良好特性及高可靠性。
- （三）惟顯示裝置之製造方法，包括上述之各層與植入技術乃是已知之公開技術，包含US 5055898、US 5166085、US 5877514、US 5989377、US 6225150、US 6225644、EP 0361609、JP A02224254、JP A60160170等，故本案係運用申請前既有之技術或知識，而為熟習該項技術者所能輕易完成，不符法定專利要件。同時，本案說明書實施例只說明方法，然而效果如何並無具體數據顯示其特性及可靠性，不具進步性，不符合法定專利要件。
- （四）檢附前述引證資料摘要（如附件）。

經濟部智慧財產局

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第二頁

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